



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,944	06/26/2003	Shigeharu Monoe	12732-158001	5033
26171	7590	07/11/2005	EXAMINER	
FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			TOLEDO, FERNANDO L	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/603,944	Applicant(s) MONOE, SHIGEHARU	
	Examiner Fernando L. Toledo	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 June 2005 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (US Patent Application Publication US 2002/0158288 A1).

In re claims 1 and 7, Yamazaki, in the US Patent Application Publication US 2002/0158288 A1; figures 1A – 20 and related text, discloses forming a laminate layer comprising a lower first conductive layer 108a and an upper second conductive layer 108b over a semiconductor layer 102 with a gate insulating film 107 interposed between the semiconductor

layer and the conductive layers; forming a mask pattern 110 over the laminate layer; forming a first conductive layer pattern 117 having a tapered edge by etching the second conductive layer and the first conductive layer (Figure 1B); after forming the first conductive layer pattern, recessing an edge of the mask pattern remaining on the first conductive layer pattern (Figure 1C); after recessing the edge of the mask pattern, forming a second conductive layer pattern 124 by selectively etching the second conductive layer in the first conductive layer pattern in accordance with of the mask pattern (Figure 1C and Paragraph 0086); and forming an LDD region 130 in a region of the semiconductor layer overlapping with the first conductive layer in the second conductive layer pattern by using the second conductive layer in the second conductive layer pattern as a mask for shielding ions accelerated by an electric field (Figure 1C).

3. In re claims 2 and 8, Yamazaki discloses wherein the first conductive layer is made of tungsten, and the second conductive layer is made of aluminum or metal having aluminum as the main component (Paragraph 0081).

4. In re claims 3 and 9, Yamazaki discloses wherein the edge of the mask pattern remaining on the first conductive layer pattern is recessed by oxygen plasma treatment (Paragraph 0083).

5. In re claims 4 and 11, Yamazaki discloses forming a laminate layer over a semiconductor layer 104 by sequentially depositing a first conductive layer 108a, a second conductive layer 108b, and a third conductive layer 108c with a gate insulating film 107 interposed between the semiconductor layer and the conductive layers; forming a mask pattern 110 on the laminate layer; forming a first conductive layer pattern 117 having a tapered edge; after forming the first conductive layer pattern, recessing an edge of the mask pattern remaining on the first conductive layer pattern; after recessing the edge of the mask pattern, forming a second conductive layer

Art Unit: 2823

pattern by selectively etching the third conductive layer and the second conductive layer in the first conductive layer pattern on the in accordance with basis of the mask pattern (Figure 1C and Paragraphs 0085 – 0086); and forming an LDD 130 region in a region of the semiconductor layer overlapping with the first conductive layer in the second conductive layer pattern by using the third conductive layer and the second conductive layer in the second conductive layer pattern as a mask for shielding ions accelerated by an electric field (Figure 1C).

6. In re claim 5, Yamazaki discloses wherein the first conductive layer is made of tungsten, the second conductive layer is made of aluminum or alloy or compound having aluminum as the main component, and the third conductive layer is made of titanium nitride (Paragraph 0082).

7. In re claims 6 and 12, Yamazaki discloses wherein the edge of the mask pattern remaining on the first conductive layer pattern is recessed by oxygen plasma treatment (Paragraph 0083).

8. In re claims 10 and 13, Yamazaki discloses wherein the width of the mask pattern is decreased by plasmas treatment using a fluorine-based etch (Paragraph 0083).

Response to Arguments

9. Applicant's arguments filed 21 June 2005 have been fully considered but they are not persuasive for the following reasons.

10. Applicant argues that Yamazaki does not disclose recessing an edge of the mask pattern remaining on the first conductive layer pattern after forming the first conductive layer pattern. Examiner respectfully submits that the recessing of the edge of the mask pattern is the mask used to form a second conductive layer pattern and hence the mask pattern has to be recessed in the

Art Unit: 2823


first etching processing and the second etching process is used to pattern the second conductive pattern as it is disclosed on Paragraphs 0083 – 0086 of the Yamazaki reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Thu 7am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Fernando L. Toledo
Examiner
Art Unit 2823

flt
8 July 2005